



### G83/2 Appendix 4 Type Verification Test Report

Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2.			
SSEG Type reference number		Photovoltaic Grid-tied inverter	
SSEG Type		X1-0.7-S-D/X1-0.7-S-N	
System Supplier name		Solax power Co., Ltd	
Address		Room 220, West Buliding A, National University Science and Technology Park of Zhejiang University 525, Xixi Rd, Hangzhou, Zhejiang Province, China, 310007	
Tel	+86(0571)-56260011	Fax	+86(0571)-56075753
E:mail	info@soalxpower.com	Web site	www.solaxpower.com
Maximum rated capacity, use separate sheet if more than one connection option.	Connection Option		
	0.7	kW single phase system	
	NA	kW single phase system	
	NA	kW single phase system	
	NA	kW two phases in three phase system	
	NA	kW two phases split phase system	
SSEG manufacturer/supplier declaration. I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.			
Signed	<i>Guo Huawei</i>	On behalf of	Solax power Co., Ltd
Note that testing can be done by the manufacturer of an individual component, by an external test house, or by the supplier of the complete system, or any combination of them as appropriate. Where parts of the testing are carried out by persons or organisations other than the supplier then the supplier shall keep copies of all test records and results supplied to them to verify that the testing has been carried out by people with sufficient technical competency to carry out the tests.			



**Power Quality. Harmonics.** The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1

SSEG rating per phase (rpp)		0.7	kW		NV=MV*3.68/rpp	
Harmonic	At 50% of rated output		100% of rated output		Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps		
2	0.018	0.095	0.017	0.089	1.080	
3	0.024	0.126	0.031	0.163	2.300	
4	0.009	0.047	0.009	0.047	0.430	
5	0.043	0.226	0.048	0.252	1.140	
6	0.006	0.032	0.008	0.042	0.300	
7	0.026	0.137	0.014	0.074	0.770	
8	0.005	0.026	0.006	0.032	0.230	
9	0.019	0.100	0.019	0.100	0.400	
10	0.003	0.016	0.004	0.021	0.184	
11	0.013	0.068	0.012	0.063	0.330	
12	0.003	0.016	0.003	0.016	0.153	
13	0.011	0.058	0.009	0.047	0.210	
14	0.002	0.011	0.003	0.016	0.131	
15	0.008	0.042	0.007	0.037	0.150	
16	0.002	0.011	0.004	0.021	0.115	
17	0.006	0.032	0.006	0.032	0.132	
18	0.002	0.011	0.002	0.011	0.102	
19	0.004	0.021	0.006	0.032	0.118	
20	0.001	0.005	0.002	0.011	0.092	
21	0.004	0.021	0.004	0.021	0.107	
22	0.001	0.005	0.002	0.011	0.084	
23	0.003	0.016	0.003	0.016	0.098	
24	0.001	0.005	0.001	0.005	0.077	
25	0.003	0.016	0.004	0.021	0.090	
26	0.001	0.005	0.001	0.005	0.071	
27	0.002	0.011	0.002	0.011	0.083	
28	0.001	0.005	0.001	0.005	0.066	
29	0.002	0.011	0.002	0.011	0.078	
30	0.001	0.005	0.001	0.005	0.061	
31	0.002	0.011	0.002	0.011	0.073	
32	0.002	0.011	0.002	0.011	0.058	
33	0.001	0.005	0.001	0.005	0.068	
34	0.002	0.011	0.002	0.011	0.054	
35	0.001	0.005	0.001	0.005	0.064	
36	0.002	0.011	0.002	0.011	0.051	
37	0.001	0.005	0.001	0.005	0.061	
38	0.003	0.016	0.003	0.016	0.048	
39	0.002	0.011	0.002	0.011	0.058	
40	0.004	0.021	0.003	0.016	0.046	

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.



<b>Power Quality. Voltage fluctuations and Flicker.</b> The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3								
X1-0.7-S-D/X1-0.7-S-N								
	Starting			Stopping			Running	
	$d_{max}$	$d_c$	$d_{(t)}$	$d_{max}$	$d_c$	$d_{(t)}$	$P_{st}$	$P_{it}$ 2 hours
Measured Values	0.48	0.43	0	0.36	0.28	0	0.08	0.08
Normalised to standard impedance and 3.68kW for multiple units	NA	NA	NA	NA	NA	NA	NA	NA
Limits set under BS EN 61000-3-3	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65
Test start date	2016-04-12			Test end date			2016-04-12	
Test location	Building 4, No. 518, Xinzhuan Road, Caohejing Songjiang High-Tech Park, Shanghai, P.R. China (201612)							

<b>Power quality. DC injection.</b> The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4			
X1-0.7-S-D/X1-0.7-S-N			
Test power level	10%	55%	100%
Recorded value	19mA	13mA	10mA
as % of rated AC current	0.62%	0.42%	0.32%
Limit	0.25%In or 20mA	0.25%In or 20mA	0.25%In or 20mA
<p>The effects of, and therefore limits for, <b>DC</b> currents injected in the <b>DNO's Distribution System</b> is an area under current investigation by <b>DNOs</b>. Until these investigations are concluded the upper limit for <b>DC</b> injection is 0.25% of <b>AC</b> current rating per phase. Where a <b>SSEG</b> is designed to be installed singly in an installation, for example a domestic CHP unit, then this <b>DC</b> injection limit can be a maximum value of 20mA for sub 2kW <b>SSEG</b> and can be tested alone,. Where <b>SSEGs</b> are designed such that multiple units may be installed in an installation for example roof mounted wind turbines and PV with micro <b>Inverters</b> on each panel, then they should be tested as a group of at least 2kW and with a maximum group size of 4kW. Tests are to be carried out a three power levels plus or minus 5%.</p>			

<b>Power Quality. Power factor.</b> The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2			
X1-0.7-S-D/X1-0.7-S-N			
	216.2V	230V	253V
Measured value	0.991	0.991	0.989
Limit	>0.95	>0.95	>0.95

Measured at three voltage levels and at full output. Voltage to be maintained within  $\pm 1.5\%$  of the stated level during the test.



<b>Protection. Frequency tests</b> The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3						
X1-0.7-S-D/X1-0.7-S-N						
Function	Setting		Trip test		"No trip tests"	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20s	47.5HZ	20.5s	47.7Hz 25s	No trip
U/F stage 2	47Hz	0.5s	47.01HZ	0.560s	47.2Hz 19.98s	No trip
					46.8Hz 0.48s	No trip
O/F stage 1	51.5Hz	90s	51.5HZ	93.3s	51.3Hz 95s	No trip
O/F stage 2	52Hz	0.5s	52.01HZ	0.533s	51.8Hz 89.98s	No trip
					52.2Hz 0.48s	No trip

<b>Protection. Voltage tests</b> The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						
X1-0.7-S-D/X1-0.7-S-N						
Function	Setting		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s	200.1V	2.56s	204.1V 3.5s	No trip
U/V stage 2	184V	0.5s	184.4V	0.549s	188V 2.48s	No trip
					180V 0.48s	No trip
O/V stage 1	262.2V	1.0s	262.2V	1.03s	258.2V 2.0s	No trip
O/V stage 2	273.7V	0.5s	273.7V	0.992s	269.7V 0.98s	No trip
					277.7V 0.48s	No trip

Note for Voltage tests the Voltage required to trip is the setting  $\pm 3.45V$ . The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting  $\pm 4V$  and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

<b>Protection. Loss of Mains test.</b> The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4						
X1-0.7-S-D/X1-0.7-S-N						
Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.						
Test Power and imbalance	33% -5% Q Test 22	66% -5% Q Test 12	100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5s	0.194S	0.196S	0.200S	0.174S	0.172S	0.420S



**Protection. Frequency change, Stability test** The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6

X1-0.7-S-D/X1-0.7-S-N				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

**Protection. Re-connection time.** The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5

X1-0.7-S-D/X1-0.7-S-N					
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.					
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
30 s	59.9 s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		No-reconnection	No-reconnection	No-reconnection	No-reconnection

**Fault level contribution.** The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6

X1-0.7-S-D/X1-0.7-S-N					
For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	$i_p$	NA	20ms	159 V	3.02 A
Initial Value of aperiodic current	$A$	NA	100ms	NA	NA
Initial symmetrical short-circuit current*	$I_k$	NA	250ms	NA	NA
Decaying (aperiodic) component of short circuit current*	$i_{DC}$	NA	500ms	NA	NA
Reactance/Resistance Ratio of source*	$X/R$	NA	Time to trip	8.7 ms	In seconds

**Self-Monitoring solid state switching** The requirement is specified in section 5.3.1, No specified test requirements.

X1-0.7-S-D/X1-0.7-S-N		Yes/or NA
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds.		NA

Additional comments